REMARKS

Reconsideration and withdrawal of the rejections set forth in the Office Action are respectfully requested. In that Office Action, Claims 12-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,734,055 to Lin et al. ("Lin").

In the Office Action, the Examiner indicates that Lin includes L-shape dielectric layer (referring to FIG. 3 Lin). Applicant disagrees with this characterization of Lin. Applicant has carefully reviewed FIG. 3 of Lin and the L-shape dielectric layer mentioned by the Examiner is not found in the prior art. There is no description relating to the L-shape dielectric layer in the Lin. As seen in page 11, lines 10-16 of the present specification, the L-shape structure according to the present invention is formed on the sidewall of the gate. The L-shape structure includes a vertical portion attached on the sidewall of the gate and a lateral portion (where tunneling occurs) formed on the substrate.

The dielectric layer 180 is attached onto the gate. Applicant believes that the layer 180 is the L-shape dielectric layer mentioned by the Examiner. The layer 180 attached on the gate sidewall is not L-shape; rather, it is more similar to a U-shape and the layer 180 surrounds the gate. Further, in the claimed invention, the lateral portion is formed under the spacer 206a that is used for trapping charge (page 11, lines 14) and it is the region where tunneling occurs. There is no equivalent structure in Lin. Indeed, the lateral portion of Lin's U-shape structure 180 is under the control gate 195, where tunneling cannot take place.

Regarding the rejection of claims 14-15, the Examiner notes the table shown in Lin. In the table of Lin, there are only two doped regions consisting of a source and drain. There is a limitation of third and forth doped region in the claimed invention, respectively. Therefore, Lin fails to teach the programming method of the third and forth doped region. Further, claims 14-15 include a limitation of third bit or fourth bit, respectively. However, Lin's structure is two-bits only. See col. 7, lines 18-20. Lin fails to anticipate the step of programming third or forth bit.

Regarding the rejection of claims 16-17, the claimed invention discloses the L-shape dielectric layer that is not disclosed by Lin as mentioned above. In the claimed invention, the erasing voltage is

applied on the gate and first (or second) doped region. However, in the table and description of col. 7, lines 12-17 of Lin, the control gate is biased negatively while source and drain positively. Therefore, Lin fails to anticipate the claimed invention that limits the erasing mode by applying erasing voltage on the gate and first (or second) doped region.

Regarding the rejection of claims 18-19, the claimed invention discloses the L-shape dielectric layer that is not disclosed by Lin as mentioned above. In the claimed invention, the reading voltage is applied on the gate and first (or second) doped region. The reading bias level is lower than the voltage applied during programming for sensing the channel current. By carefully review of Lin, these is no suggestion indicated that the reading bias level is lower than the voltage applied during programming. Further, Lin also does not anticipate the step of sensing the channel current to determine the binary status in the spacers, as mentioned in claims 18-19. Therefore, Lin fails to anticipate the claimed invention.

Regarding the rejection of claim 20, the claimed invention discloses the L-shape dielectric layer that is not disclosed by Lin as mentioned above. In the claimed invention, the binary status is removed by exposing the memory to a UV environment. Lin does not disclose the feature of the claimed invention. Examiner also fails to show that Lin teaches this aspect of the present invention. Therefore, Lin fails to anticipate the claimed invention.

In view of the foregoing, the claims pending in the application comply with the requirements of 35 U.S.C. § 102 and are patentable over the citation of Lin. A Notice of Allowance is, therefore, respectfully requested.

Applicant encloses a one-month extension fee. However, if any additional fees are due, please charge our Deposit Account No. 50-0665, under Order No. 386998017US1 from which the undersigned is authorized to draw.

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Respectfully submitted,

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